REMARKS

The last Office Action in the above-identified application and the reference cited by the Examiner have been carefully considered. Claims 1 and 2 have been amended in a sincere effort to define more clearly and more specifically features of Applicant's invention which distinguish over the art of record.

In the last Office Action, Claims 1 through 4 were rejected as being anticipated by U.S. Patent No. 6,297,085 (Aoki, et al.), and Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatenable over the Aoki, et al. patent. This rejection is respectfully traversed, especially in light of the amendments to the claims submitted herewith.

The Aoki, et al. patent discloses a method for manufacturing a ferroelectric capacitor and method for manufacturing a ferroelectric memory. The Examiner particularly refers to Figure 17 of the Aoki, et al. patent for showing a ferroelectric memory which has an insulation film 40, a concave portion 12, a lower electrode layer 6 and an upper electrode layer 18. The Examiner also contends that the Aoki, et al. patent discloses a film 20 formed in the bottom of the concave portion 12.

To clarify the distinguishing features of the invention set forth in the subject application, Claims 1 and 2 have been amended. In particular, Claim 1, which has been thrice amended, now more specifically defines the ferroelectric memory as having a lower electrode layer wherein a portion of only the lower electrode layer is embedded in the concave portion and protrudes outwardly from the inner peripheral edge of the insulation film which forms the concave portion. Also, Claim 2, which has now been twice amended, more specifically defines the memory as including another film which is embedded from the top [illegible] depth, this film being exposed

at a bottom of the hollow and separating the insulation film from the lower electrode layer in the hollow, and now furthermore specifically defines this film as being an etch stop for forming the hollow to the predetermined depth.

First, with respect to twice amended Claim 2, it is respectfully requested that the Examiner refer to Figure 9 of the drawings of the subject application. The embodiment defined by amended Claim 2 is exemplified by Figure 9 of the drawings. In accordance with Claim 2, the memory includes a film 38 embedded from the top surface of the first insulation film 12 in a position of a predetermined depth. This film 38 is exposed at the bottom of the hollow 24, and separates the first insulation film 12 from the lower electrode 16 in the hollow 24. The film 38 is specifically defined in twice amended Claim 2 as being an etch stop for forming the hollow 24 to said predetermined depth. The purpose, of course, of film 38 is to prevent the further etching of the insulation film 12 below the predetermined depth in order to form the hollow 24.

In Figure 17 of the Aoki, et al. patent, there is a contact hole 12, a lower electrode 6, an insulating layer 40 and a barrier layer 20. The barrier layer is not an etch stop. The Aoki, et al. patent specifically describes the inclusion of the barrier layer 20 so as "to prevent diffusion of the constitutive elements of the capacitor (please see Column 4, lines 23-26 of the Aoki, et al. patent). This barrier layer does not act as an etch stop, and no further etch stop is described in the Aoki, et al. patent. Accordingly, Claim 2, as now more specifically amended, patentably distinguishes over the Aoki, et al. patent and is respectfully urged to be allowable.

Claim 1 now more specifically defines the ferroelectric memory as where only the [illegible] subject application) is embedded in the

hollow (concave portion) 14 at the top surface of the first insulation film 12. Because of this, the top surface of the upper electrode 20 may be made flat. This allows the ferroelectric memory and its constituent laminated layers to be highly integrated.

As clearly shown in Figure 17 of the Aoki, et al. patent, not only does the lower electrode 6 reside in the contact hole 12, but also the PZT film 17 and the upper electrode 18 are embedded in the contact hole at the top surface of the SiO_2 insulating layer 40. It is respectfully pointed out that the upper electrode 18 of the Aoki, et al. patent is not made flat over the area of the contact hole 12. Accordingly, it is respectfully urged that Claim 1, as now more specifically amended, patentably distinguishes over the Aoki, et al. patent and is allowable.

Claim 3, in its present form, defines the ferroelectric memory as including an insulation film having a hollow, and a laminated body having a lower electrode layer, a ferroelectric layer formed on the lower electrode layer and an upper electrode layer formed on the ferroelectric layer. Claim 3 specifically defines the lower electrode layer as including a first electrode portion formed at a corner of the hollow and a second electrode portion formed on the first electrode portion.

To facilitate an understanding of the embodiment defined by Claim 3, reference is respectfully made to Figure 10 of the subject application. In Figure 10, it is shown that the first electrode portion 16a may be formed at the corner of the hollow 14 so that the second electrode portion 16b may be formed to provide generally the lower electrode 16. As disclosed on page 10, lines 6-19 of the subject application, with this particular structure, if the second electrode portion 16b is formed by a spin coat process, the amount of depression [illegible] the second electrode portion 16b may be

decreased when the lower electrode 16 is baked. Also, if the second electrode portion 16b or the first conductive film 26b is formed by sputtering, the variation in the crystalline orientation may be reduced in the top surface of the lower electrode 16. This latter embodiment is shown in Figure 11 of the subject application. This serves to stabilize the crystalline state of the ferroelectric 18 which is formed on the lower electrode 16.

It is respectfully urged that the Aoki, et al. patent does not disclose the structural features set forth in Claim 3 of the subject application. As shown in Figure 17 of the Aoki, et al. patent, the lower electrode 6 is formed of a single layer, and the thin film 20 is not a lower electrode, but rather is a barrier layer, as mentioned previousiy. There is no lower electrode layer formed of a first electrode portion (such as 16a) and formed at a corner of the hollow and a second electrode portion (such as 16b) formed on the first electrode portion. As such, it is respectfully urged that Claim 3 patentably distinguishes over the Aoki, et al. patent and is allowable.

Claim 4 specifically calls for a ferroelectric memory having an insulation film with a concave portion, and a laminated body having a lower electrode layer which is brought into contact with a bottom surface of the concave portion, a thin film of the same material as that of the lower electrode layer formed on the surface of the lower electrode layer, a ferroelectric layer formed on the thin film and an upper electrode layer formed on the ferroelectric layer, and further wherein a side of the thin film, the ferroelectric layer and the upper electrode layer are flush with each other.

The embodiment defined by Claim 4 is shown by way of example in Figure 8 of the subject application. The thin film 36 shown in Figure 8 is made from the same material as [illegible] the thin film 36 being formed on the

planarized first conductive film 26. The advantage of having a thin film 36 formed on the surface of the planarized first conductive film 26 and using for the thin film 36 the same material of the first conductive film 26 is that it eliminates the surface roughening in the first conductive film which is caused by the planarization process. This is disclosed at page 9, lines 17-20 of the subject application.

In contrast, the Aoki, et al. patent shows in Figure 17 that no layer is formed between the lower electrode 6 and the PZT film 17. Even more specifically, not only is no layer shown between lower electrode 6 and the PZT film 17, but there is no disclosure in the Aoki, et al. patent to provide such a film which would be formed from the same material as the lower electrode 6. Accordingly, it is respectfully urged that the Aoki, et al. patent does not teach or suggest the structural features set forth in Claim 4.

Claim 5, in its present form, defines the ferroelectric memory as having an insulation film having a concave portion, and a laminated body having a lower electrode layer, a ferroelectric layer formed on the lower electrode layer and an upper electrode layer formed on the ferroelectric layer. Claim 5 specifically defines the lower electrode layer and the insulation film at their respective top surfaces as being planarized flush with each other, and further defines a side of the ferroelectric layer and a side of the upper electrode layer as being flush with each other.

Reference is made specifically to Figure 7 of the drawings of the subject application, for an example of the structure which is defined by Claim 5. As shown in Figure 7, the top surfaces of the first conductive film (i.e., the lower electrode) 26 and the insulation film 12 are planarized flush with each other. Because of this, the etch time can be even further

shortened, because there is no need to etch the first conductive film 26 portion extending out of the hollow 14, as none exists.

The Aoki, et al. patent does not show the lower electrode and the insulation film being planarized flush, such as shown in Figure 7 and defined by Claim 5 of the subject application. As shown in Figure 2D of the Aoki, et al. patent, the top surfaces of the lower electrode 6 and the insulating layer 1 are not planarized flush with each other. Thus, the structure of the Aoki, et al. ferroelectric capacitor would not lead to a shortened etch time, which would result from the structure set forth in Claim 5 of the subject application. Accordingly, it is respectfully urged that the Aoki, et al. patent does not teach or suggest the particular structure of the ferroelectric memory set forth in Claim 5.

In summary, it is respectfully urged that Claims 1 and 2, as more specifically amended, and Claims 3-5, in their present form, patentably distinguish over the Aoki, et al. patent and are allowable.

In view of the foregoing amendments and remarks, entry of the amendments to Claim 1 and 2, reconsideration of unamended Claims 3-5 and allowance of the application with Claims 1-5 are respectfully solicited.

Respectfully submitted,

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VERSION OF AMENDMENT WITH MARKS TO SHOW CHANGES MADE

IN THE CLAIMS:

1. (Thrice Amended) A ferroelectric memory, comprising:

an insulation film having a concave portion at a top surface; and

a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said concave portion, wherein said laminated body includes a lower electrode layer which is brought into contact with a bottom surface of said concave portion, a ferroelectric layer formed on said lower electrode layer and an upper electrode layer formed on said ferroelectric layer, wherein a portion of said lower electrode layer is only embedded in said concave portion, and protrudes outward from an inner peripheral edge forming said concave portion, and a side of said portion of said lower electrode layer, a side of said ferroelectric layer and a side of said upper electrode layer are flush with each other.

2. (Twice Amended) A ferroelectric memory, comprising:

an insulation film having a hollow at a top surface; and

a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said hollow, wherein said laminated body includes a lower electrode layer, a ferroelectric layer formed on said lower electrode layer and an upper electrode layer formed on said ferroelectric layer; and the memory further comprising [a] another film [formed in] embedded from said top surface [of said] film in a position of a predetermined depth, exposed at a bottom of said

hollow and separating between said insulation film and said lower electrode layer in said hollow, said another film being an etch stop for forming the hollow to said predetermined depth.